PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Zhao et al.	)	Group Art Unit: 2811
Serial No.: 09/317,536	)	Examiner: Douglas W. Owens
Filed: May 24, 1999	)	Docket No. 50324-1170
For: Interconnect With Low Dielectric Constant Insulators For Semiconductor Integrated Circuit Manufacturing	)	

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SECOND RESPONSE TO FINAL OFFICE ACTION

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The Final Office Action mailed October 24, 2001 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

AUTHORIZATION TO DEBIT ACCOUNT

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to deposit account no. 20-0778.

AMENDMENTS

Please substitute the following clean copy text for the pending claims of the same number:

16. (Once Amended) An interconnect comprising:

(a) one or more metal lines formed from a first metal layer, said metal lines having gaps therebetween;

(b) low-k material filling the gaps between the metal lines and having a height and one or more vertical portions;

(c) a protective layer formed over the metal lines and the low-k material, wherein the protective layer covers at least one vertical portion of the low-k material.

(d) a dielectric layer formed over the protective layer, wherein the dielectric layer has a different composition than the low-k material;

(e) one or more vias etched in the dielectric layer;

(f) a metal for filling the vias;

(g) a second metal layer formed over the dielectric layer; and

(h) one or more openings in the protective layer for allowing the metal vias to contact the first metal lines.

28. (Twice Amended) An interconnect structure comprising:

a plurality of metal lines formed on a substrate;

low-k dielectric structures interposed between two or more of said metal lines;

a second dielectric material formed above said metal lines, wherein portions of said second dielectric material are formed between portions of said low-k dielectric structures;

a protective layer interposed between said low-k dielectric structures and said second dielectric material, wherein said protective layer is configured to provide etch selectivity between said protective layer and said second dielectric material; and

a conductive feature formed within said second dielectric material and said protective layer, said conductive feature in contact with at least one of said plurality of metal lines.